

Appl. No. 09/802,291

Amdt. dated April 15, 2005

Reply to Office Action of January 26, 2005

PATENT**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A processing core that executes a compare instruction, the processing core comprising:
 - a plurality of general-purpose registers comprising a first input operand register, a second input operand register and an output operand register;
 - a register file comprising the plurality of general-purpose registers;
 - comparison logic coupled to the register file, wherein:
 - the comparison logic tests for at least two of ~~the~~ a following relationships with the compare instruction alone: less than, equal to, greater than or no valid relationship,
 - the comparison logic with the compare instruction alone produces a value, and
 - the value has at least three states to represent ~~the~~ at least two of ~~the~~ following relationships: less than, equal to, greater than or no valid relationship;
 - decode logic, which selects the output operand register from the plurality of general-purpose registers; and
 - a store path between the comparison logic and the selected output operand register, wherein the value is stored in the selected output operand register.
2. (Original) The processing core that executes the compare instruction as set forth in claim 1, wherein a very long instruction word includes a plurality of compare instructions.

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3. (Previously Presented) The processing core that executes the compare instruction as set forth in claim 1, wherein said decode logic selects the first and second input operand registers from the plurality of general-purpose registers.

4. (Original) The processing core that executes the compare instruction as set forth in claim 1, wherein the processing core issues a plurality of compare instructions at one time.

5. (Previously Presented) The processing core that executes the compare instruction as set forth in claim 1, further comprising:
a first load path between the first input operand register and the comparison logic;
and
a second load path between the second input operand register and the comparison logic.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The processing core that executes the compare instruction as set forth in claim 1, wherein the value is an integer.

9. (Original) The processing core that executes the compare instruction as set forth in claim 1, wherein:
the first input operand register is a double precision floating point data type;
the second input operand register is a single precision floating point data type; and
the output operand register is a double precision floating point data type.

10. (Original) The processing core that executes the compare instruction as set forth in claim 1, further comprising a plurality of processing paths that are coupled to the register file.

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11. (Original) The processing core that executes the compare instruction as set forth in claim 1, wherein the register file comprises special purpose registers which cannot store an output operand.

12. (Currently Amended) A method for performing a compare operation, the method comprising steps of:

decoding a compare instruction;

configuring first and second paths between a register file and comparison logic;

configuring a third path between the comparison logic and the register file;

comparing a first input operand and a second input operand with the compare operation alone ~~to~~, wherein the comparing step comprises step of:

producing a result, which has at least three states to indicates at least two of ~~the~~ a following mathematical relationships between the first input operand and the second input operand: less than, equal to, greater than, or no valid relationship; and

coupling the result to a general-purpose register in the register file.

13. (Original) The method for performing the compare operation as set forth in claim 12, the method further comprising a step of enabling the comparison logic in an arithmetic logic unit.

14. (Original) The method for performing the compare operation as set forth in claim 12, wherein the configuring steps each comprise a step of addressing a general-purpose register in the register file.

15. (Previously Presented) The method for performing the compare operation as set forth in claim 12, wherein a compare operation is comprised within a very long instruction word.

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16. (Previously Presented) The method for performing the compare operation as set forth in claim 12, wherein the comparing step comprises a step of converting a data type of at least one of the first or second input operands.

17. (Currently Amended) A method for executing a compare instruction in a processor, the method comprising steps of:
issuing the compare instruction;
comparing a first input operand and a second input operand to determine at least two mathematical relationships between the first and second input operands, wherein the compare instruction alone causes the comparing step;
determining an output operand which has at least three states indicative of the at least two mathematical relationships; and
storing the output operand in a general-purpose register of a register file, wherein the output operand alone indicates the at least two mathematical relationships between the first and second input operands.

18. (Previously Presented) The method for executing the compare instruction in the processor as set forth in claim 17, wherein the comparing step comprises at least two of the following steps:
determining if the first input operand is less than the second input operand;
determining if the first input operand is greater than the second input operand;
determining if the first input operand is equal to the second input operand; or
determining if there is no valid relationship between the first input operand and the second input operand.

19. (Original) The method for executing the compare instruction in the processor as set forth in claim 17, wherein the compare instruction is a very long instruction word which comprises a plurality of compare instructions which are processed in parallel down separate processing paths.

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20. (Original) The method for executing the compare instruction in the processor as set forth in claim 17, wherein the general-purpose register is used to store operators from other types of instructions.

21. (Previously Presented) The processing core that executes the compare instruction as set forth in claim 1, wherein the value in the operand register can be written to a location outside of the processing core.

22. (Previously Presented) The method for performing the compare operation as set forth in claim 12, wherein the result can be written to a location outside of the processing core.